



Attorney's Docket No.: 42P16680

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In Re Patent Application of: )

Justin K. Brask et al. )

Application No.: 10/750,061 )

Filed: December 30, 2003 )

For: NONPLANAR TRANSISTORS WITH )  
METAL GATE ELECTRODES )

Examiner: Lindsay Jr., Walter Lee

Art Unit: 2812

Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

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Sir:

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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 10/12, 2005

  
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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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**Complete if Known**

Application Number	10/750,061
Filing Date	December 30, 2003
First Named Inventor:	Justin K. Brask et al.
Art Unit	2812
Examiner Name	Lindsay Jr., Walter L.
Attorney Docket Number	42P16680

**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (If known)				
		US-	6,709,982 B1	03/23/2004	Buynoski et al.	
		US-	6,645,797 B1	11/11/2003	Buynoski et al.	
		US-	6,475,869 B1	11/05/2002	Yu	
		US-	5,545,586	08/13/1996	Koh	
		US-	2004/0256647 A1	12/23/2004	Lee et al.	
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		US-	2002/0036290 A1	03/28/2002	Inaba et al.	
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**FOREIGN PATENT DOCUMENTS**

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		Country Code <sup>3</sup>	Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
		EP	1 202 335 A	05/02/2002	IBM	Page 6, par 22	
		JP	2002298051	10/17/2003	Lee Soko	Abstract, Fig 11	

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**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
		BURENKOV, A. et al., "Corner Effect in Double and Triple Gate FINFETs", European Solid-State Device Research, 2003 33 <sup>rd</sup> Conference on Essderc '03 September 2003, Piscataway, NJ, USA, IEEE, pages 135-138, XP010676716	
		CHANG, S.T. et al, "3-D Simulation of Strained Si/SiGe Heterojunction FinFETS", Semiconductor Device Research Symposium, 2003 International, December 2003, Piscataway, NJ, USA, IEEE, pages 176-177, XP010687197	
		International Search Report PCT/US2005/010505	

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